A Generic Model of Memristors With Parasitic Components

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***Abstract*—In this paper, a generic model of memristive systems, which can emulate the behavior of real memristive devices is proposed. Non-ideal *pinched hysteresis loops* are sometimes observed in real memristive devices. For example, the hysteresis loops may deviate from the origin over a broad range of amplitude A and frequency f of the input signal. This deviation from the ideal case is often caused by parasitic circuit elements exhibited by real memristive devices. In this paper, we propose a *generic memristive circuit model* by adding four *parasitic circuit elements*, *namely*, a small capacitance, a small inductance, a small DC current source, and a small DC voltage source, to the memristive device. The adequacy of this model is verified experimentally and numerically with two thermistors (NTC and PTC) memristors.**

***Index Terms*—Generic model, memristive devices, memristor, parasitic components, pinched hysteresis loop.**

I. Introduction

THE DISCOVERY of a physical model of a TiO_2 memristor [1] by a team of scientists from *hp* has attracted enormous interests from both industry and academia. The memristor was originally postulated by Leon Chua as the fourth basic circuit element in electrical circuits [2]–[4], and generalized in 1976 to a broader class of dynamical systems called memristive devices [5]. The most distinguished feature of memristive devices is the "*pinched hysteresis loop*" on *i-v* plane for any bipolar periodic voltage or current input signal that has a zero average value. Consequently, pinched hysteresis loops are used as the *fingerprint* to identify memristive devices. An "*ideal*" pinched hysteresis loop must pass through origin for any bipolar periodic input voltage $v(t)$ [resp., input current $i(t)$], which assumes both positive and negative voltages (resp., currents) and has a zero mean. The shape of the pinched hysteresis loop varies with frequency f and shrinks to a single-valued function through the origin, as the frequency tends to infinity [6].

Another fingerprint of a memristor is the dependency of pinched hysteresis *lobe area* on the frequency f of the periodic excitation signal. Beyond some critical frequency f_c, the area of each of the two pinched hysteresis lobes in the first and third quadrant decreases monotonically as the frequency of the periodic input voltage $v(t)$ [resp., current $i(t)$] increases.

Although pinched hysteresis loops are the fingerprints of memristive devices, experimentally-measured pinched hysteresis loops of some real "*physical*" memristive devices may not pass through the origin [7]–[11], [20], [21]. In some cases, the pinched point may even disappear beyond some frequency f of the applied voltage source $v(t)$, or current source $i(t)$ [7]. Also crucial impact of parasitic components may appear on the modeling the dynamics of log domain circuits [19]. Similarly, intelligence of the plasmodia and slime mould can be mapped to LC contour with a memristor [22], [23]. Fig. 1 shows some examples of experimentally measured non-zero crossing pinched hysteresis loops from real memristive devices, such as plants, Physarum, TiO_2-based metal insulator devices, redox-based resistive switches, electrochemical systems, and venus fly trap [7]–[10], [20], [21]. The non-zero location of the pinched point may be caused by the presence of parasitic circuit elements and/or batteries.

The goal of this paper is to show, how to derive a composite 1-port circuit model $\mathcal{M}$ as shown in Fig. 2, which can emulate the *measured* pinched loops over a broad range of amplitude A and frequency f, as closely as possible.

The concept of a "model" implies that there is no *exact* model for real-world devices [12]. In this paper, we propose a simple tractable 1-port memristor circuit model with a *memristor* plus *four-small* circuit elements, called parasitics, that can emulate the experimental pinched hysteresis loops as closely as possible over a set $[A, f]$ of amplitude A and frequency f. Our proposed model can be applied to any memristive device whose measured pinched hysteresis loop did not pass through the origin [10], [20] where the *pinched point* occurs *near* the origin. The effect of the DC voltage source and/or current source is to *translate* this pinched point to the origin.

This paper is organized as follows: Section II reviews the characteristic fingerprints of an ideal memristor and memristive system. Section III presents our *generic* memristor circuit model using a memristor, a parasitic capacitance, a parasitic inductance, a small DC current source, and a small DC voltage source.

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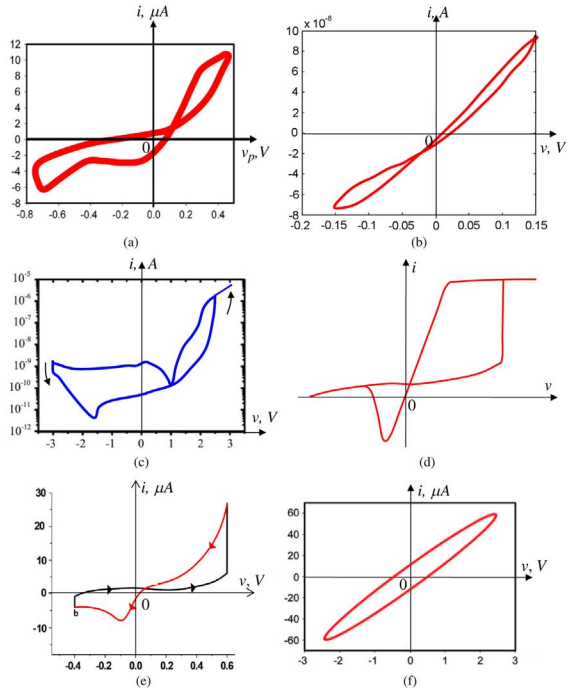

Fig. 1. Examples of non-zero crossing pinched hysteresis loops measured from some physical and organic memristors. (a) Memristor in plants [7]. (b) Slime mould memristors [8]. (c) TiO_2 based metal-insulator-metal devices [9]. (d) Nanobatteries in redox based switches [10]. (e) Electrochemical systems [20]. (f). Memristors in the venus flytrap [21].

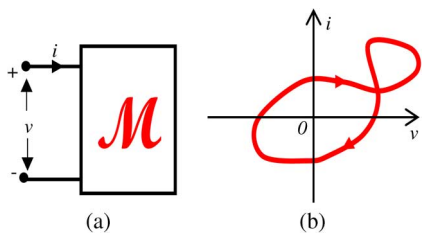

Fig. 2. (a) Composite 1-port circuit model $\mathcal{M}$ of a memristor-like device. (b) Illustration of a non-zero crossing pinched hysteresis loop.

Section IV describes our generic memristor circuit model of an NTC thermistor, and a PTC thermistor. Comparison between the experimental and the simulated results from our generic NTC and PTC thermistor models are presented in Section V. Finally, some concluding remarks are presented in Section VI.

II. Fingerprints of Memristors

A memristor is defined as a two-terminal electrical device whose instantaneous voltage and current obey the *state-dependent Ohm's law*. In this paper, we consider *current-controlled memristors* defined by

$$\left.\begin{aligned} v &= M(x_1, x_2, \ldots, x_n)i \\ \tfrac{dx_k}{dt} &= f_k(x_1, x_2, \ldots, x_n; i), \quad k = 1, 2, \ldots, n \end{aligned}\right\} \tag{1}$$

where M is a continuous function of $(x_1, x_2, \ldots, x_n)$, called the *memristance*, and x_i's are the "n" *state variables* defined by a system of "n" ordinary differential equations.

Similarly, we consider *voltage-controlled memristors* defined by

$$\left.\begin{aligned} i &= W(x_1, x_2, \ldots, x_n)v \\ \tfrac{dx_k}{dt} &= f_k(x_1, x_2, \ldots, x_n; v), \quad k = 1, 2, \ldots, n \end{aligned}\right\} \tag{2}$$

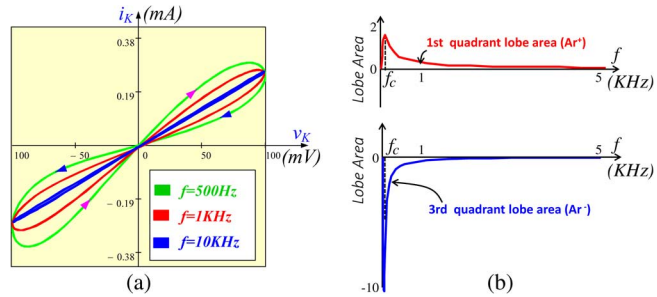

Fig. 3. Fingerprints of a memristor. (a) Zero-crossing (passing through origin) pinched hysteresis loop shrinks continuously as frequency f increases. It will tend to a straight line as f tends to infinity. (b) The absolute value of each lobe area decreases as the frequency of the input signal increases for $f > f_c$.

where W is a continuous function of the n state variable $(x_1, x_2, \ldots, x_n)$, called the *memductance*.

A fingerprint of memristor is the zero-crossing pinched hysteresis loops on the *current* i *versus voltage* v plane under any bipolar *zero-mean*, sine wave-like excitations. Another fingerprint is the change in shape of the pinched hysteresis loop with the frequency f. In particular, it shrinks to a single-valued function through the origin, as the frequency tends to infinity. Fig. 3(a) shows an example of the pinched hysteresis loops of the first-order generic memristor for frequencies, $0 \leq f \leq \infty$, [13]–[15], [17].

Another fingerprint of memristor is the dependency of the hysteresis lobe area on the frequency of the periodic excitation. For a bipolar periodic input voltage $v(t)$, or current $i(t)$, the pinched hysteresis loop has a typical shape depending on the memristor constitutive relation. Above a certain critical frequency f_c, the magnitude of the area of the hysteresis lobe in the 1st or 3rd quadrant is inversely proportional to the excitation frequency f. This property asserts that, the magnitude of the area of the pinched lobe gradually decreases with increasing frequency for $f > f_c$, as shown in Fig. 3(b) for a memristor. The lobe area computed using *Riemann-Stieltjes integral* tracks the orientation of pinched hysteresis loop in clockwise or counterclockwise direction [15]. If the lobe area is positive (resp., negative) during a half cycle of the input signal, then the orientation of the pinched loop is clockwise (resp., counterclockwise) either in the 1st quadrant, or the 3rd quadrant, respectively and vice versa. The 1st and 3rd quadrant *lobe area vs. frequency* curve shown in Fig. 3(b) for a memristor is positive and negative respectively, which illustrate that the orientation of pinched hysteresis loop is clockwise and counterclockwise respectively.

III. Generic Memristor Device Model

Our generic memristor device model is shown in Fig. 4. It consists of a voltage-controlled or current-controlled memristor M in parallel with a *parasitic* capacitor C_p and a *parasitic* DC current source I_P, where a *parasitic* inductor L_p in series with a *parasitic* DC voltage source E_P, is connected in series with the upper part of the circuit. The principle and circuit-theoretic concepts behind this generic circuit model date back to the mid-nineteen-sixties and had been presented at various conferences and applied in several publications on device modeling [12], [16], [18].

If v is the input voltage at time t in Fig. 4, then by KVL,

$$v = v_1 + v_2, \tag{3}$$

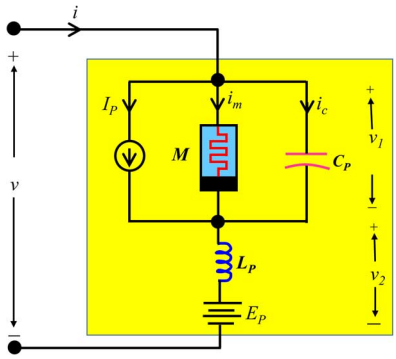

Fig. 4. Generic memristor device model.

where v_1 is the voltage across the parallel connection of M and C_P, and v_2 is the voltage across the serial connection of L_P and E_P.

The current i is given by KCL,

$$i = I_P + i_m + i_c, \tag{4}$$

where I_P, i_m, i_c denote the DC current source, the current through the memristor, and the current through the capacitor, respectively. Here, M denotes the memristance $M(x_1, x_2, \ldots, x_n)$ which depends on the state variables $(x_1, x_2, \ldots, x_n)$ of the memristor.

It follows from (3) and (4) that,

$$\frac{dv_1}{dt} = \frac{1}{C_P}\left[i - \frac{v_1}{M(x_1, x_2, \ldots, x_n)} - I_P\right] \tag{5}$$

$$\frac{di}{dt} = \frac{1}{L_P}[v - v_1 - E_P] \tag{6}$$

The state variables $(x_1, x_2, \ldots, x_n)$ are defined by "n" state equations

$$\begin{aligned}
\frac{dx_1}{dt} &= f_1(x_1, x_2, \ldots, x_n; v_1)\\
\frac{dx_2}{dt} &= f_2(x_1, x_2, \ldots, x_n; v_1)\\
&\bullet\\
&\bullet\\
&\bullet\\
\frac{dx_n}{dt} &= f_n(x_1, x_2, \ldots, x_n; v_1),
\end{aligned} \tag{7}$$

where we have assumed the memristor M is *voltage-controlled* and described by

$$i_m = \frac{1}{M(x_1, x_2, \ldots, x_n)} v_1. \tag{8}$$

Altogether, (5), (6), and (7) constitute $n + 2$ state equations in $n + 2$ state variables $(v_1, i; x_1, x_2, \ldots, x_n)$.[1] We will see in the following sections that the parasitic capacitance C_p, the parasitic inductance L_p, as well as the independent DC voltage E_P and DC current I_P can cause the *Lissajoux figure* to deviate from the origin $(v, i) = (0, 0)$.[2]

There exist many memristive devices made of "*organic*" materials or "*electrolytes*" which exhibit a *pinched* hysteresis loop where the "pinched point" occurs *near*, but not exactly at, the origin [10], [20]. Such devices are *not* passive because a small current will flow when a *passive* resistor is connected across the device. The energy in such memristive devices come from the internal chemical reactions, which can generate a small voltage, such as the classic Nernst potential.

IV. Modeling NTC and PTC Thermistors

Thermistors are physical devices whose steady-state DC resistance measured at a fixed applied DC voltage varies significantly with changes in the device *temperature*, which is a *state variable* whose dynamics is determined by some differential equation involving the state variable, and the input voltage.

1) Generic Memristor Circuit Model for a Physical NTC Thermistor: An ideal voltage-controlled, *negative-temperature-coefficient* (NTC) thermistor [5], [16] can be modeled by a voltage-controlled memristor with only one state variable $x \triangleq T_N$:

$$i_N = W(T_N) v_N, \tag{9}$$

$$W(T_N) = \left(R_{0N} e^{\beta_N \left(\frac{1}{T_N} - \frac{1}{T_{0N}}\right)}\right)^{-1} \tag{10}$$

where v_N and i_N denote respectively the terminal voltage and current of the NTC thermistor, $W(T_N)$ denotes the temperature-dependent conductance of the NTC thermistor, R_{ON} denotes the thermistor resistance at ambient temperature T_{0N}, T_N denotes a *single* state variable x_1 in (7) representing the absolute temperature of the NTC thermistor, and β_N denotes a material-specific constant. Observe that the conductance $W(T_N)$ of the NTC thermistor with respect to T_N in (10) increases as the temperature T_N increases. Hence, the resistance $R(T_N) \triangleq 1/W(T_N)$ decreases as T_N increases.[3] The state variable (temperature) T_N depends on the power dissipation of the device via the *heat balance equation*,

$$\frac{dT_N}{dt} = \frac{\delta_N}{H_{CN}}(T_{0N} - T_N) + \frac{W(T_N)}{H_{CN}} v_N^2, \tag{11}$$

where δ_N denotes the dissipation constant, and H_{CN} denotes the heat capacitance of the NTC thermistor.

In this paper, we will model a real *physical* NTC thermistor using the generic memristor device model in Fig. 4 via the three state (5), (6), and (7), with $E_P = 0$ and $I_P = 0$:

State equations describing a "*physical*" NTC thermistor

$$\frac{dv_1}{dt} = \frac{1}{C_P}\left[i - \frac{v_1}{\left(R_{0N} e^{\beta_N \left(\frac{1}{T_N} - \frac{1}{T_{0N}}\right)}\right)} - I_P\right] \tag{12}$$

$$\frac{di}{dt} = \frac{1}{L_P}[v - v_1 - E_P] \tag{13}$$

$$\frac{dT_N}{dt} = \frac{\delta_N}{H_{CN}}(T_{0N} - T_N) + \frac{W(T_N)}{H_{CN}} v_1^2. \tag{14}$$

2) Generic Memristor Circuit Model for a Physical PTC Thermistor: An ideal voltage-controlled *positive-temperature-*

[1]Observe that the state variable v_1 in (5) is just the voltage across the *parasitic capacitor* C_P. Similarly, the state variable i in (6) is just the current through the *parasitic inductor* L_P.

[2]For many real memristive devices, such as thermistors, the parasitic voltage source E_P and the parasitic current source I_P are negligible and can be set to zero.

[3]The NTC thermistor is said to be a "*negative-temperature dependent*" resistor because its resistance *decreases* as the temperature increases. The subscript "N" of v, i, and T in (9)–(11) pertains to a "*negative-temperature dependent*" resistor.

coefficient (PTC) thermistor is usually modeled with only one state variable $x \triangleq T_P$:

$$i_P = W(T_P)v_P \tag{15}$$

$$W(T_P) = \left(R_{0P}e^{\beta_P(T_P - T_{0P})}\right)^{-1} \tag{16}$$

$$\frac{dT_P}{dt} = \frac{\delta_P}{H_{CP}}(T_{0P} - T_P) + \frac{W(T_P)}{H_{CP}}v_P^2 \tag{17}$$

where v_p and i_p denote respectively the terminal voltage and current of the PTC thermistor, $W(T_P)$ denotes the conductance of the PTC thermistor, R_{OP} denotes the thermistor resistance at ambient temperature T_{0P}, T_P denotes a single state variable (absolute temperature) x_1 in (7), β_P denotes a material-specific constant, δ_P denotes the dissipation constant and H_{CP} denotes the heat capacitance of the PTC thermistor. Observe from (16) that when the absolute temperature T_P increases, then conductance $W(T_P)$ of the PTC thermistor decreases. Hence, the resistance $R(T_P) \triangleq 1/W(T_P)$ increases as T_P increases.[4]

In this paper, we will model a real *physical* PTC thermistor using the generic memristor device model in Fig. 4 via the three state (5), (6), and (7), with $E_P = 0$, and $I_P = 0$:

Stateequationsdescribinga "*physical*" PTCthermistor

$$\frac{dv_1}{dt} = \frac{1}{C_P}\left[i - \frac{v_1}{\left(R_{0P}e^{\beta_P(T_P - T_{0P})}\right)} - I_P\right] \tag{18}$$

$$\frac{di}{dt} = \frac{1}{L_P}[v - v_1 - E_P] \tag{19}$$

$$\frac{dT_P}{dt} = \frac{\delta_P}{H_{CP}}(T_{0P} - T_P) + \frac{W(T_P)}{H_{CP}}v_1^2. \tag{20}$$

V. Experimental and Simulation Results

In this section, we present hardware experiments and numerical simulations of negative-temperature coefficient (NTC) and positive-temperature coefficient (PTC) thermistors. The hardware experiments were performed with commercially available NTC and PTC thermistors at room temperature and their results were compared with simulations from our generic memristor device model.

The ideal mathematical models of NTC and PTC thermistors defined in (9)–(11) and (15)–(17) were simulated with a sinusoidal voltage source $v(t) = A\ \sin(2\pi ft)$ of amplitude A and frequency f. The parameters used for the NTC and PTC thermistors in this paper are:

NTC thermistor: $T_{0N} = 300$ K, $R_{0N} = 3.89$ KΩ, $H_{CN} = 0.14$ J/K, $\delta_N = 0.1$ W/K, $\beta_N = 5 \times 10^5$ K,

PTC thermistor: $T_{0P} = 300$ K, $R_{0P} = 40\ \Omega$, $H_{CP} = 0.6$ J/K, $\delta_P = 0.05$ W/K, $\beta_P = 2$ K.

Fig. 5(a) and Fig. 5(b) show the numerically calculated pinched hysteresis loops of the NTC and the PTC thermistors at different frequencies of the applied sinusoidal voltage source (with amplitude $A = 6$ V). Observe that, the loci in the *current vs. voltage* plane for the input signal exhibits zero-crossing pinched hysteresis loops for all the frequencies, as expected. Observe that the shape and lobe area of the pinched hysteresis

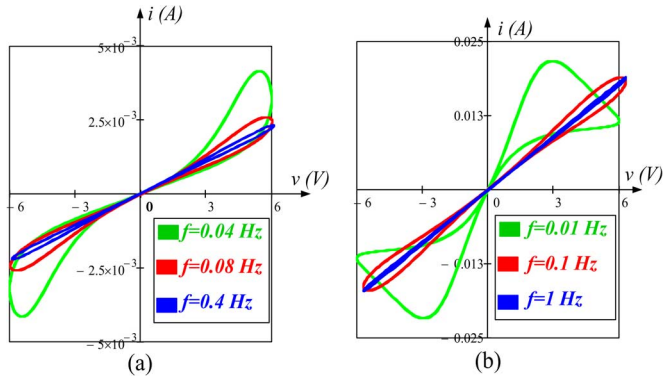

Fig. 5. Zero-crossing pinched hysteresis loops of ideal mathematical models of (a) NTC, and (b) PTC thermistors at different frequencies. The input is a sinusoidal voltage source with amplitude $A = 6$ V.

loops shrink as the frequency of the input signal increases as expected. All pinched hysteresis loops of the ideal mathematical model of the NTC and the PTC thermistors satisfy the required fingerprints of a memristor, as expected.

Hardware experiments were conducted on both NTC and PTC thermistors to validate our generic memristive device model for real memristive devices. The first experiment was conducted on a commercially available *Thermometric's-NTC thermistor*[5] in our laboratory. The initial small-signal resistance of the NTC thermistor was measured with an Ohm meter at zero DC applied voltage to be equal to 3.89 KΩ at room temperature. Fig. 6 shows the experimental results measured with the NTC thermistor driven by a sinusoidal voltage source with amplitude $A = 5$ V at different frequencies. When the frequency f of the input signal is varied from 0.01 Hz to 100 Hz, the oscilloscope displays pinched hysteresis loops which pass through the origin. However, as the frequency of the input signal increases beyond 1 KHz, the pinched hysteresis loops on *i-v* plane did *not* pass through the origin and the shape of the pinched loops also changes as the frequencies of the input signal increases. Fig. 6 also shows the simulation results of the NTC thermistor, when it is modeled with the generic memristor device model. The same input (sinusoidal source with amplitude $A = 5$ V) is used in both tables. The parameters used for the simulation is $C_P = 5$ nF, $L_P = 2$ mH, $E_P = 0$ V, $I_P = 0$ A. Observe that the experimental results (shown in *blue*) obtained from the NTC thermistor in the left side of each table is similar to the simulation results (shown in *red*) in the right side of the corresponding table, in Fig. 6.

In order to see the role played by the parasitic capacitor C_P and parasitic inductor L_P, Fig. 7 shows the corresponding results when only (9)–(11) (without the parasitic C_p and L_p) are used for simulation, instead of the generic memristor device model. Comparing Fig. 6 and Fig. 7, we observe that the parasitics play an increasing role as the frequency increases beyond 100 Hz.

Fig. 8 shows simulation of the NTC thermistor when the effect of a parasitic voltage source E_P, and a parasitic current source I_P are non-zero, and C_P and L_P are zero. When NTC

[4]The PTC thermistor is said to be a "*positive-temperature dependent*" resistor because its resistance *increases* as the temperature increases. The subscript "P" of v, i, and T in (15)–(17) pertains to a "*positive-temperature dependent*" resistor.

[5]The experiment was performed at lab environment on glass coated NTC Diode thermometrics thermistors (NTC-3.896KGJG). The device can be purchased and its specifications can be found from the following websites: http://www.devicemart.co.kr/goods/view.php?seq=8598, http://www.ge-mcs.com/download/temperature/920-320C.pdf.

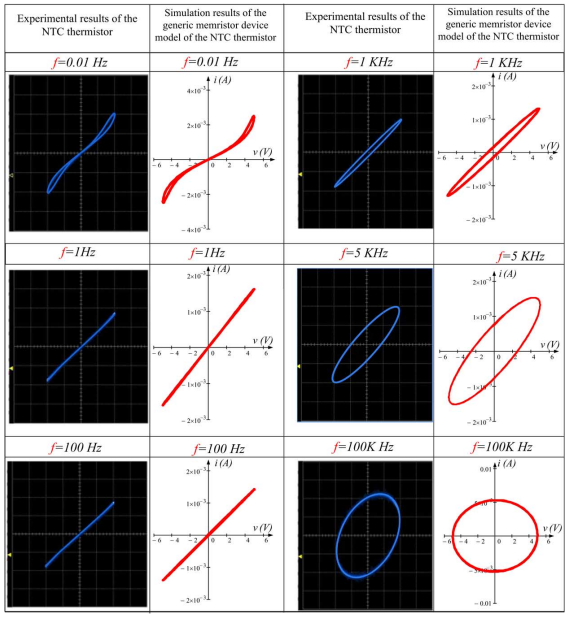

Fig. 6. Experimental measurements (*blue*) of a commercially available Thermometric's-NTC thermistor (left side) and the corresponding simulated results (*red*) using the generic memristor device model (right side). The input is a sinusoidal source with amplitude of $A = 5$ V. The experiment on the NTC thermistor was conducted at room temperature. The *scale* of i and v on the left side of each table is identical to that shown on the right side. The parameters used for simulations of the generic memristor device model of the NTC thermistor are: $T_{0N} = 300$ K, $R_{0N} = 3.89$ KΩ, $H_{CN} = 0.14$ J/K, $\delta_N = 0.1$ W/K, $\beta_N = 5 \times 10^5$ K, $C_P = 5$ nF, $L_P = 2$ mH, $E_P = 0$ V, $I_P = 0$ A.

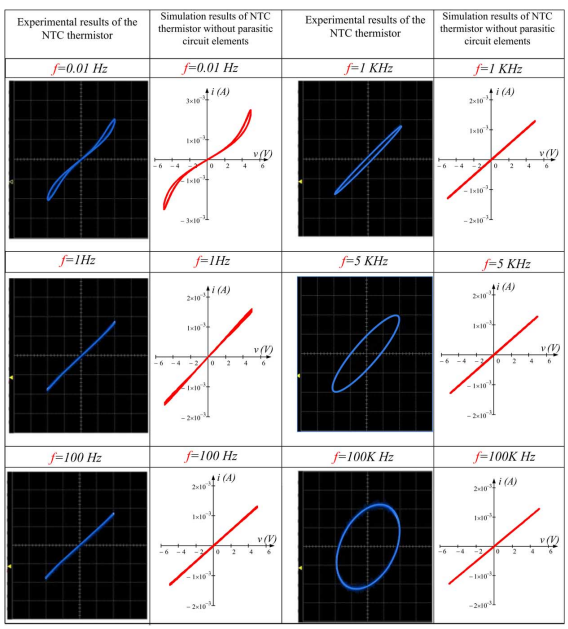

Fig. 7. Simulated results using (9)–(11) (without parasitics) corresponding to Fig. 6.

is driven by a sinusoidal source with amplitude $A = 6$ V at frequencies $f = 0.1$ Hz and 0.3 Hz, the pinched hysteresis loops are not only translated to the pinched point but the shape of the pinched loops also changes as the value of E_P and I_P are varied. However, for higher frequencies $f = 100$ Hz, the $i - v$ curve of the NTC thermistor is unchanged in shape except a translation to the point (E_P, I_P).

In order to see the effects of non-zero parasitic circuit elements in the NTC thermistor, the simulations are performed

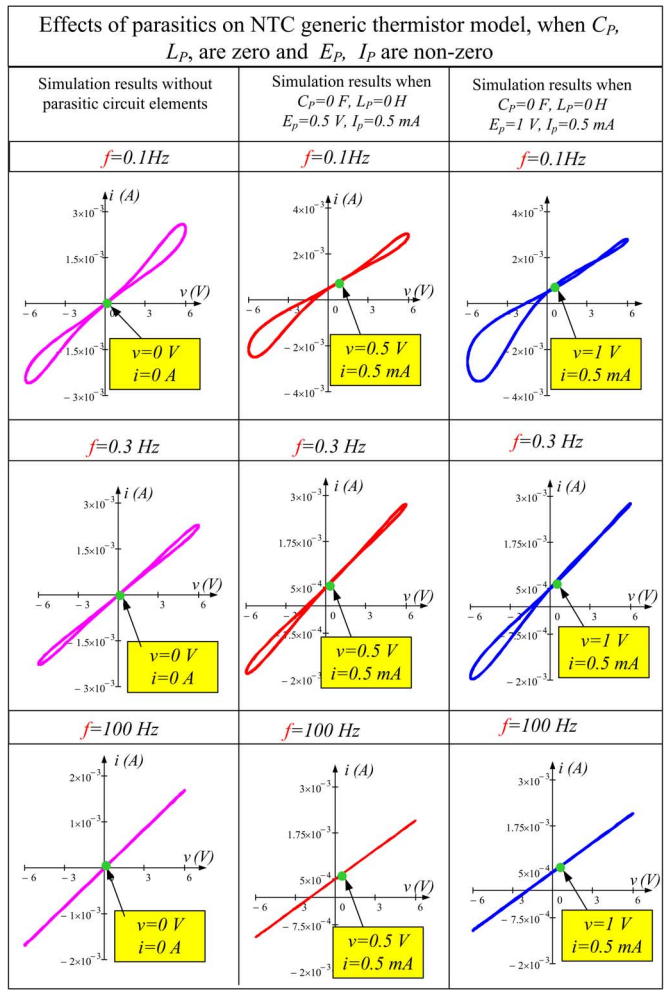

Fig. 8. Pinched hysteresis loops of the NTC thermistor *without* parasitic circuit elements (*magenta*) in column 1 and corresponding results (*red and blue*) using the generic memristor device model in columns 2 and 3. The results of NTC generic memristor device model is obtained for different values of E_P and I_P when $C_P = 0$, $L_P = 0$.

for different values of C_P, L_P, E_P, I_P at various frequencies. Fig. 9 shows the pinched hysteresis loops in the NTC generic memristor device corresponding to frequencies $f = 0.08$ Hz, 1 Hz, and 10 KHz for sinusoidal source with amplitude A = 6 V. Observe that the pinched hysteresis loops are changed to different shapes depending on the values of non-zero parasitic components.

We performed experiments on a commercially available *Murata's-PTC thermistor*.[6] The small-signal initial resistance at $v = 0$ was measured with an Ohm meter to be equal to 40 Ω, at room temperature. Fig. 10 shows the experimental and simulation results of the PTC thermistor using the PTC generic memristor device model for input voltage $v_p = Asin(2\pi ft)$ with $A = 5$ V, at different frequencies. The parameters used for the simulation are: $C_P = 0.1$ μF, $L_P = 0.2$ mH, $E_P = 0$ V,

[6]The experiment was performed at lab environment on Murata's Lead type PTC thermistors (PTFM04BE471Q2N34B0). The device can be purchased and its specifications can be found from the following websites: http://www.eleparts.co.kr/EPXANC6G, http://search.murata.co.jp/Ceramy/CatalogAction.do?sHinnm =PTH9M04BE471TS2F333&sNHinnm=PTFM04BE471Q2N34B0&sNhin_key= PTFM04BE471Q2N34B0&sLang= en&sParam= PTFM04BE471Q2N34B0.

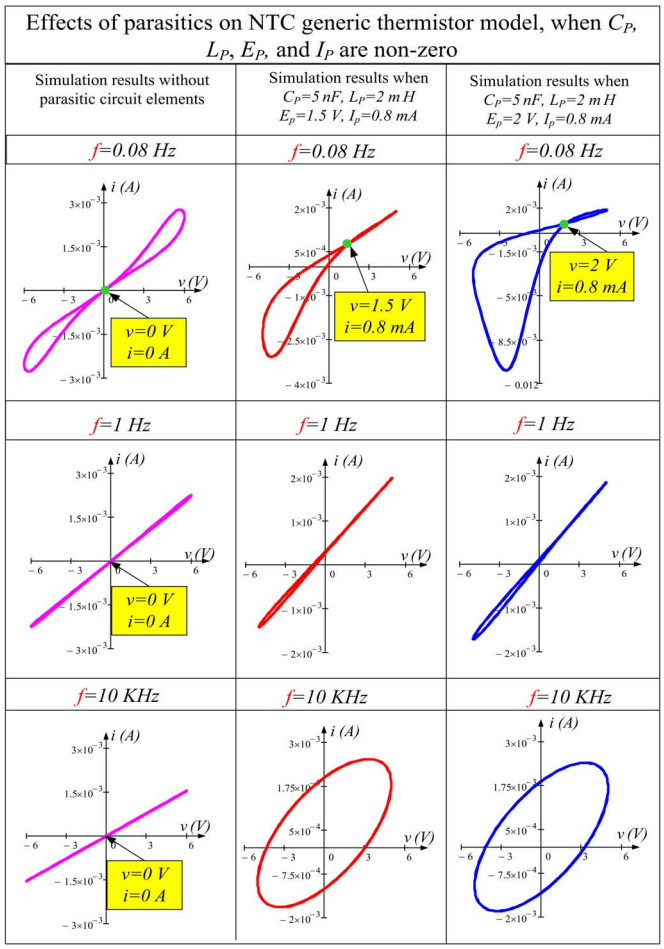

Fig. 9. Pinched hysteresis loops of the NTC memristor *without* parasitic circuit elements (*Magenta*) in column 1 for sinusoidal input $v = A\sin(2\pi ft)$ $(A = 6$ V), and corresponding results (*red and blue*) in columns 2 and 3 using the generic memristor device model. The results of the NTC generic memristor device model is obtained for non-zero values of C_P, L_P, E_P and I_P.

$I_P = 0$ A. Observe that at low frequencies, the pinched hysteresis loops on the $i - v$ plane are pinched at the origin. However, the loops are not pinched at higher frequencies. Observe that the experimental results (shown in *blue*) obtained from the PTC thermistor in the left side of each table is similar to the simulation results (shown in *red*) in the right side of the corresponding table in Fig. 10.

In order to see the role played by the parasitic capacitor C_P and parasitic inductor L_P, Fig. 11 shows the corresponding results when only (15)–(17) (without the parasitic C_p and L_p) are used for simulation, instead of the generic memristor device model. Observe that the parasitics play an increasing role as the frequency increases beyond 100 Hz.

Simulations are also performed in PTC generic memristor device to analyze the effects of C_P and L_P with zero and non-zero parasitic voltage source E_P and parasitic current source I_P. Fig. 12 shows the pinched hysteresis loops corresponding to different values E_P, I_P when C_P and L_P are zero. Observe that the pinched point and shape of the hysteresis loops are changed depending on the values of E_P and I_P. At $f = 0.01$ Hz *and* 0.2 Hz, the parasitic voltage E_P and parasitic current I_P play an important role in not only shifting the pinched point to

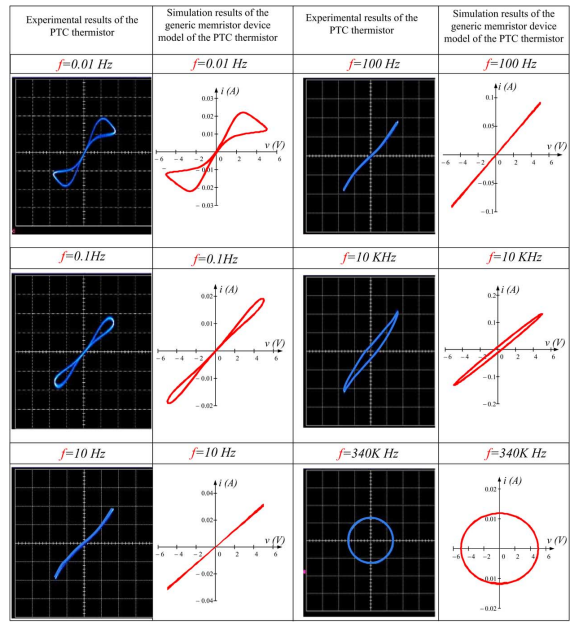

Fig. 10. Experimental measurement (*blue*) of a commercially available Murata's-PTC thermistor (left side) and the corresponding simulated result (*red*) using the generic memristor device model (right side). The input is a sinusoidal source with amplitude of $A = 5$ V. The experiment on the PTC thermistor was conducted at room temperature. The *scale* of i and v on the left side of each table is identical to that shown on the right side. The parameters used for simulations of the generic memristor device model of the PTC thermistor are: $T_{0P} = 300$ K, $R_{0P} = 40\ \Omega$, $H_{CP} = 0.6$ J/K, $\delta_P = 0.05$ W/K, $\beta_P = 2$ K, $C_P = 0.1\ \mu$F, $L_P = 0.2$ mH, $E_P = 0$ V, $I_P = 0$ A.

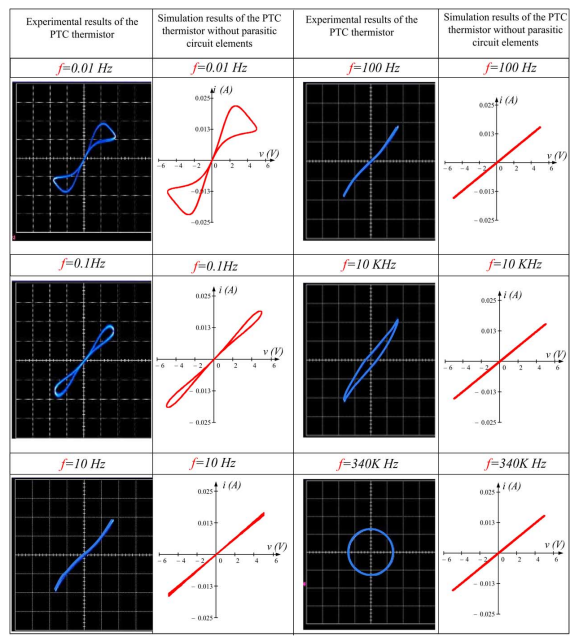

Fig. 11. Simulated results using (15)–(17) (without parasitics) corresponding to Fig. 10.

$(V, I) = (E_P, I_P)$, but also *changing* the *shape* of pinched hysteresis loops, as illustrated in Fig. 11. However at higher frequency $f = 100$ Hz, the pinched point is translated *without* changes in shape.

Simulations are also performed in PTC generic memristor device for non-zero parasitic circuit elements at different frequencies. Fig. 13 shows the pinched hysteresis loops

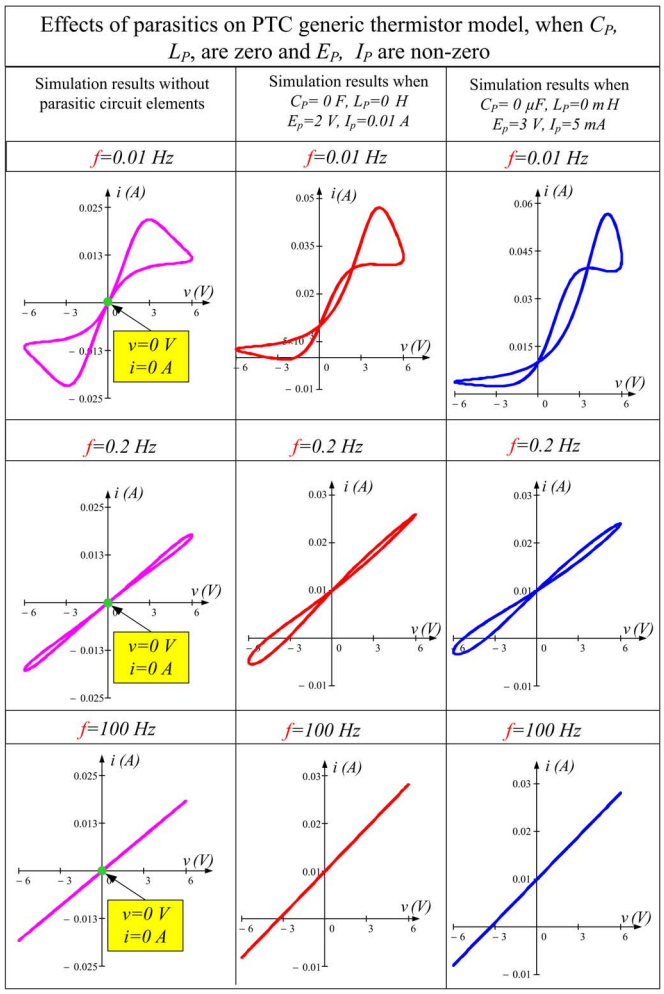

Fig. 12. Pinched hysteresis loops of the PTC thermistor *without* parasitic circuit elements (*magenta*) in column 1 and corresponding results (*red and blue*) using the generic memristor device model in columns 2 and 3. The results of PTC generic memristor device model is obtained for different values of E_P and I_P when $\mathrm{C}_P = 0$, $L_P = 0$.

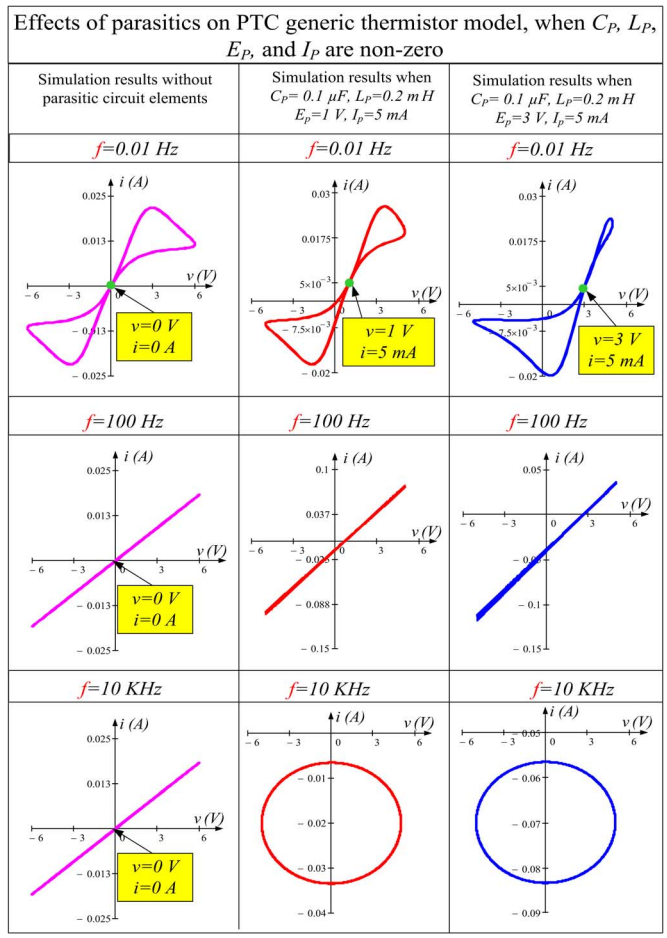

Fig. 13. Pinched hysteresis loops of the PTC memristor *without* parasitic circuit elements (*magenta*) in column 1 for sinusoidal input $v = A\sin(2\pi ft)$ $(A = 6\ \mathrm{V})$, and corresponding results (*red and blue*) in columns 2 and 3 using the generic memristor device model. The results of the PTC generic memristor device model is obtained for non-zero values of C_P, L_P, E_P, and I_P.

for input $v = Asin(2\pi ft)$ $(A = 6\ \mathrm{V})$ at frequencies $f = 0.01$ Hz, 100 Hz, and 10 Hz. Observe that, the pinched hysteresis loops are deviated and changes to different shapes depending on the values of parasitic components.

VI. Conclusion

The *pinched point* and the *shape* of the "*pinched hysteresis loop*" of real physical memristive devices may vary over a broad range of amplitude A and frequency f. In this study, a generic model of a real memristor device is proposed to emulate the behavior of real memristor devices. It is shown that the changed of the pinched hysteresis loops of a memristive system from the ideal operation can be emulated by introducing appropriate parasitic circuit elements. The experimentally measured and numerically simulated pinched hysteresis loops of the NTC and the PTC thermistors illustrate that our generic model is adequate for emulating real physical memristve devices.

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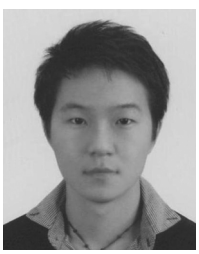

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Prof. Chua received many awards including the first recipient of the Gustav Kirchhoff award, the Guggenheim Fellow award, and the European EC Marie Curie Fellow award. He was elected a foreign member of the Academia Europaea and of the Hungarian Academy of the Sciences. He was elected Confrerie des Chevaliers du Tastevin in 2000.